A Phenomenologically Based Transient SPICE Model for Digitally Modulated RF Performance Characteristics of GaAs MESFETs

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***Abstract*—A phenomenologically based transient SPICE model was developed for GaAs MESFETs. The model accounts for both trapping and detrapping effects; hence, it can simultaneously simulate low-frequency dispersion and gate–lag characteristics. This is different from conventional models, which can simulate either effect, but not both. The present model has been used to describe both surface- and substrate-related trapping phenomena in epitaxial or ion-implanted MESFETs. The model was experimentally verified in terms of pulsed *I–V* characteristics and pulsed ac response.**

***Index Terms*—Charge carrier processes, digital modulation, MESFETs, modeling, pulse measurements, signal analysis, SPICE, transient analysis.**

I. Introduction

FOR EFFICIENT design of RF power amplifiers in digitally modulated wireless applications, it is important to develop a large-signal transistor model that is capable of predicting the device behavior over a wide range of time scales and biasing conditions. Since a general model, which accounts for all past state variables, is too cumbersome to be useful, approximation and simplification are necessary. To date, low-frequency dispersion models have been developed [1] to account for the differences between RF and dc characteristics of GaAs MESFETs. However, this type of model neglects the transient effects of digital modulation.

The transient response of MESFETs at approximately 1 μs and longer are mainly due to surface and substrate traps [2]. These traps can cause gate lag [3] in addition to low-frequency dispersion. Gate lag is associated with the *serial* events of trapping and detrapping, whereas dispersion is determined by the *average* effects of trapping and detrapping. For a given continuous wave (CW) excitation, dispersion represents the steady-state trap response as the result of a balance between trapping and detrapping. By adding simple charging and discharging subcircuits to a conventional SPICE-based MESFET model, low-frequency dispersion and gate lag can both be simulated. In [4], we described for the first time the implementation of such a model for epitaxy-based MESFETs under the influence of surface traps. This paper expands on [4] to include models for ion-implanted MESFETs and substrate traps. Using both models, pulsed ac waveforms under digital modulation were successfully simulated.

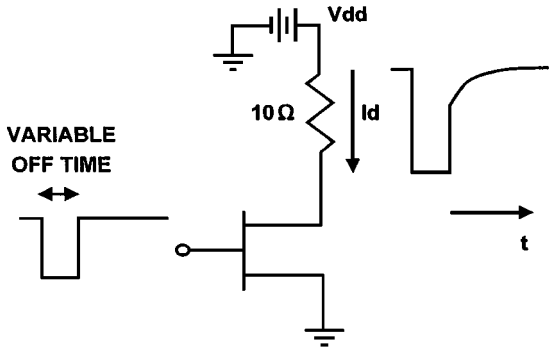

Fig. 1. Schematic of pulsed *I–V* measurement. Off times varying from microsecond to second were used to alter the trap density to various degrees. Upon returning to the quiescent point, the drain current is continuously monitored until the steady-state trap density is reestablished. The pulse repetition rate is 1 Hz for epitaxial MESFETs and 0.05 Hz for implanted MESFETs.

II. Model Construction

The present model was extracted for two types of MESFETs: one fabricated on GaAs grown by vapor-phase epitaxy, and the other fabricated by direct ion implantation into a GaAs substrate grown by the liquid-encapsulated Czochralski method. The epitaxial MESFETs have a gate length and gatewidth of 0.3 and 300 μm, respectively. Their saturated and maximum drain currents are approximately 100 and 170 mA/mm, respectively. The threshold voltage is -1.75 V. The implanted MESFETs have a gate length and gatewidth of 0.5 and 200 μm and a threshold voltage of -2 V. Their saturated and maximum drain currents are 200 and 300 mA/mm. It has been determined that the epitaxial MESFETs are primarily affected by surface traps [5], while the implanted MESFETs suffer mostly from substrate traps [6].

Pulsed *I–V* measurement (Fig. 1) was used to characterize the two types of MESFETs. Conventional pulsed *I–V* measurement

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[7] begins from a quiescent point where a steady-state trap density is maintained. Submicrosecond pulses are then applied to probe various on states without perturbing the trap density. In the present pulsed *I–V* measurement, pulses varying from microsecond to second were used to alter the trap density to various degrees. Upon returning to the quiescent point, it takes a relatively long time to reestablish the steady-state trap density and such a transient behavior is continuously monitored until it is completely over. The pulse repetition rate used in the present measurement is determined by the longest trapping or detrapping time. For epitaxial MESFETs, a rate of 1 Hz was sufficient, while implanted MESFETs required a rate of 0.05 Hz.

Since trapping usually occurs when a MESFET is driven below pinchoff under high voltages, in the present measurement, the device is typically pulsed from on to off instead of from off to on. For an epitaxial MESFET, the measurement was repeated with on-state gate–source voltages of -0.5, 0.0, and 0.5 V, off-state gate–source voltages of -4, -3, and -2 V, and off times of 0.01, 0.1, ..., 100 ms. An implanted MESFET, however, was measured with on voltages of -1.0, -0.25, and 0.5 V, off voltages of -6, -5, -4, and -3 V, and off times of 0.01, 0.04, ..., 655, 2620 ms. From the dependencies of on and off times, the trapping and detrapping rates are inferred. It was found that, for both types of MESFETs, the instantaneous drain current $i_{\rm DS}$ can be fit to (1) as follows:

$$i_{\rm DS}\left(V_{\rm DS}, V_{\rm GS}, t, V_{\rm DS}^{\rm OFF}, V_{\rm GS}^{\rm OFF}, t_{\rm OFF}\right) = I_{\rm DS}(V_{\rm DS}, V_{\rm GS}) - \sum_J \Delta I_{\rm DS}^J\left(V_{\rm DS}, V_{\rm GS}, V_{\rm DS}^{\rm OFF}, V_{\rm GS}^{\rm OFF}\right) \cdot \left(1 - e^{-t_{\rm OFF}/\tau_C^J}\right) \cdot e^{-t/\tau_D^I} \quad (1)$$

where $I_{\rm DS}$ is the steady-state drain current, $\Delta I_{\rm DS}^J$ denotes the change of drain current due to the Jth type of traps, $t_{\rm OFF}$ is the duration spent in the off state, τ_C is the trapping time constant, t is the time after the pulse, and τ_D is the detrapping time constant. Depending on the device structure, different types of traps may have to be modeled.

A. Model for Epitaxial MESFETs

When occupied, surface traps in an epitaxial MESFET can increase surface depletion, which causes the access resistance and saturated channel current to lag behind their steady-state values, as shown in Fig. 2. Fig. 3 shows the drain current of an epitaxial MESFET as a function of time after the gate–source voltage was pulsed from 0.5 to -4 V for different durations. As many as three sets of τ_C and τ_D are required to describe the transients. On the other hand, the effects of off-state drain–source and gate–source voltages are such that they can be lumped together as a single parameter in terms of off-state drain–gate voltage. Fig. 4 shows that τ_C and τ_D are approximately constant over a wide range of off-state drain–gate voltages. Fig. 5 shows that $\Delta I_{\rm DS}^J$ is approximately a linear function of off-state drain–gate voltage. Thus, the complicated historical dependence of $i_{\rm DS}$ can be greatly simplified, making (2) sufficiently compact for circuit simulation use as follows:

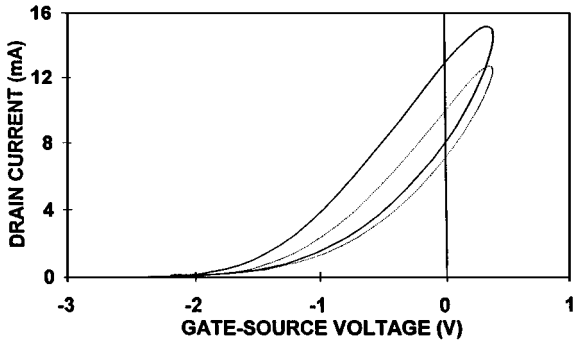

Fig. 2. Dynamic transfer characteristics of an epitaxial MESFET under a 7-kHz 1.5-V signal. Since the frequency of excitation is close to the rate of trapping, hysteresis is observed. Two sets of characteristics were measured at (—) $t = 0$ and $(\cdots)$ $t = 1$ ms, respectively, after the gate–source voltage was pulsed from -4 to -1 V. Drain supply $= 1$ V. Differences in transconductance and peak current between $t = 0$ and 1 ms are caused by detrapping.

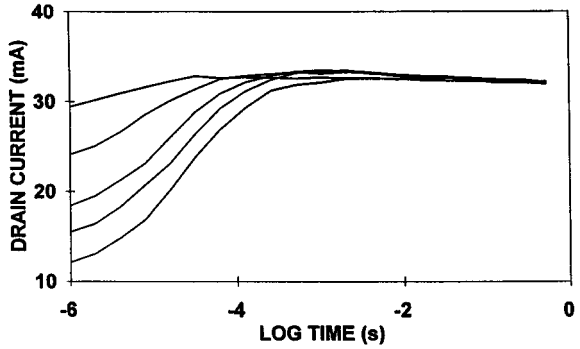

Fig. 3. Transient response of the epitaxial MESFET with time spent below pinchoff (0.01, 0.1, ...,100 ms top to bottom) as a parameter. Drain supply, on, and off gate–source voltages were equal to 1, 0.5, and -4 V, respectively. Differences in the magnitude of gate lag at $t = 0$ indicate different trapped charge densities.

$$i_{\rm DS} = I_{\rm DS}(V_{\rm DS}, V_{\rm GS}) \left[1 - \sum_{J=1,2,3} \left(\alpha_J \cdot V_{\rm DG}^{\rm OFF} + \beta_J\right) \cdot \left(1 - e^{-t_{\rm OFF}/\tau_C^J}\right) \cdot e^{-t/\tau_D^J}\right] \quad (2)$$

where α_J and β_J are fitting constants.

Using SPICE, the increase in drain resistance can be represented by a MESFET operating in the linear region, while the decrease in drain current can be represented by a voltage-dependent current source, as shown in Fig. 6(a). The parasitic MESFET and current source are controlled by a time-dependent drain–gate voltage $V'_{\rm DG}$, which is generated through a set of three nonlinear *RC* subcircuits [see Fig. 6(b)]. One subcircuit is needed for each set of trapping/detrapping times. With unity capacitance, $R_C = \tau_C$ and $R_D = \tau_D$. Diodes in the subcircuit ensure the direction of charge flow. The intrinsic MESFET can be simulated by a conventional model such as the SPICE Level 1 Curtice model extracted from steady-state drain characteristics.

B. Model for Ion-Implanted MESFETs

When occupied, substrate traps in an ion-implanted MESFET can cause the threshold voltage to shift. This can be seen in

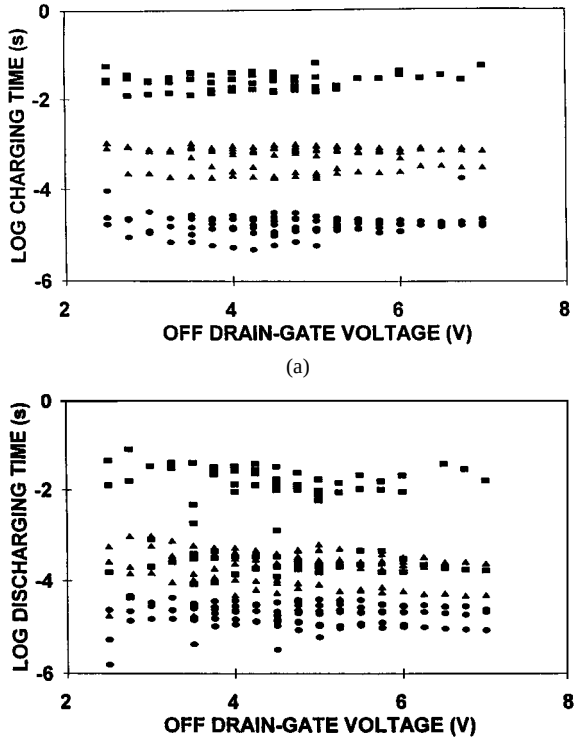

Fig. 4. Three sets of: (a) trapping and (b) detrapping time constants extracted from pulsed *I–V* characteristics of the epitaxial MESFET. The time constants are all independent of off-state drain–gate voltage. Repeated symbols at the same drain–gate voltage indicate measurements performed under different combinations of drain and gate voltages.

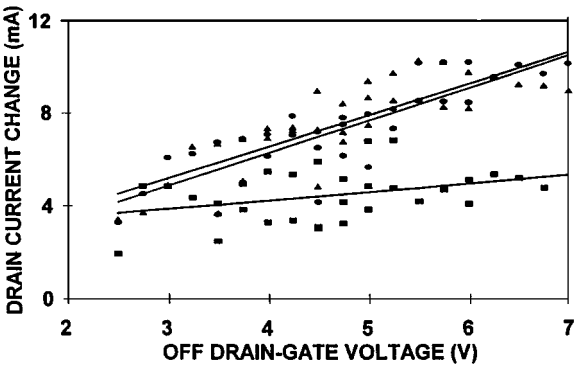

Fig. 5. Extracted drain current changes in the epitaxial MESFET, which are associated with detrapping time constants of the order of (•) microsecond, (▲) millisecond, and (■) second. On-state gate–source $= 0.5$ V.

the dynamic transfer characteristics obtained by pulsing the MESFET from two different off-state gate–source voltages, as shown in Fig. 7. Since a threshold voltage shift is difficult to implement in SPICE, its effects on the drain current is considered instead When operating in the saturated region of the MESFET drain characteristics, the resulted change in the drain current is approximately independent of the drain–source voltage. On the other hand, when operating in the linear region, the threshold shift affects mainly the channel resistance. In this case, the magnitude of the drain current transient depends on the extent to which the channel resistance affects the total drain–source series resistance. For forward gate–source biases,

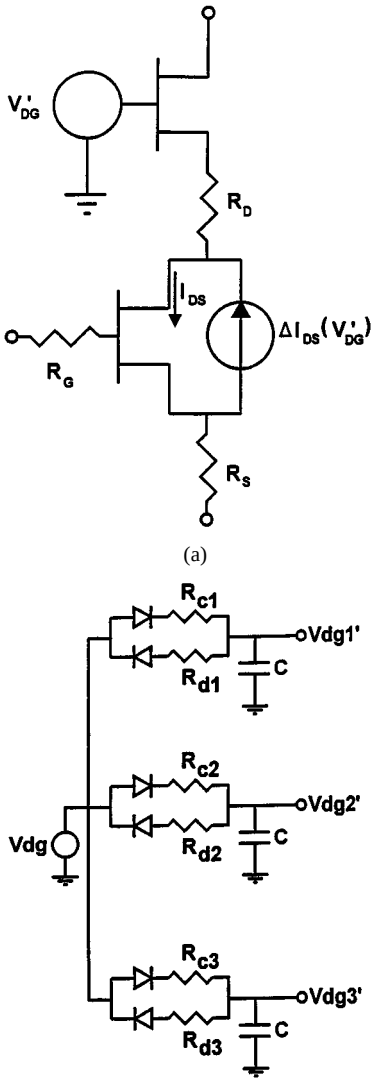

Fig. 6. Circuit model implemented in SPICE for the epitaxial MESFET. (a) Parasitic MESFET and current source are used to increase the drain resistance and decrease the saturated current, respectively. (b) Three nonlinear RC timing circuits are used to generate the voltage that controls the parasitic MESFET and current source.

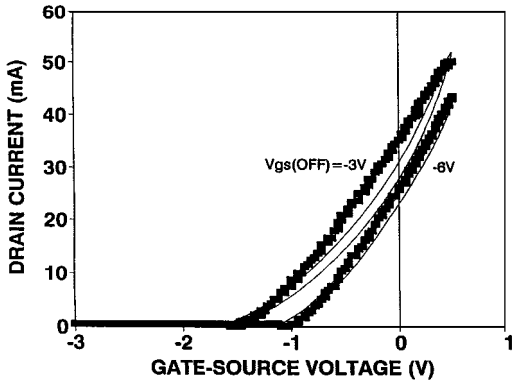

Fig. 7. Dynamic transfer characteristics of an implanted MESFET under a 100-kHz 1.75-V signal. The gate–source voltage is pulsed from either -3 to -1.25 or from -6 to -1.25 V. Shift in threshold voltage between the two cases indicate different trapping densities under different off-state gate–source voltages. (■) measured. (—) simulated.

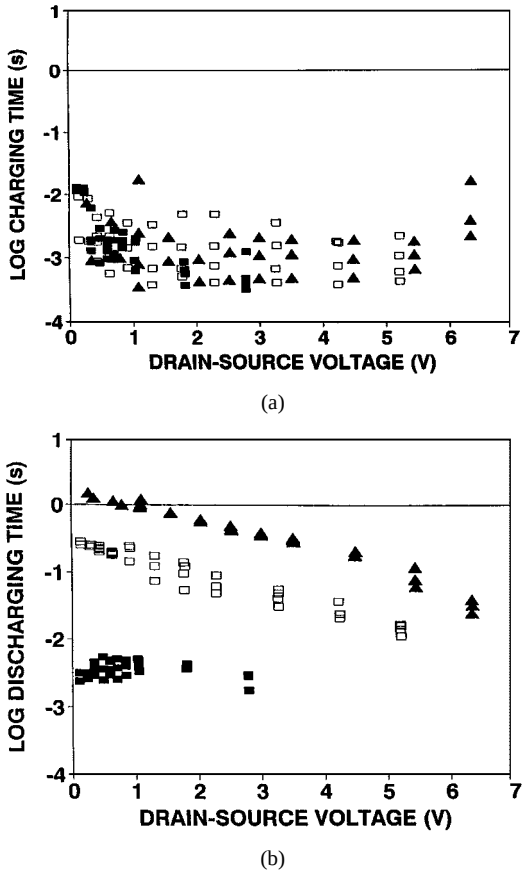

Fig. 8. (a) Trapping and (b) detrapping time constants extracted from pulsed *I–V* characteristics of the implanted MESFET. While the trapping time constants are approximately constant, the detrapping time constant varies exponentially with both on-state gate–source and drain–source voltages. On-state gate–source voltage $=$ (▲) -1.0, (□) -0.25, and (■) 0.5 V. Repeated symbols at the same drain–source voltage indicate measurements performed under different off-state gate–source voltages.

the series resistance is dominated by the access resistance and the drain current transient is reduced.

For the ion-implanted MESFET, only one set of τ_C and τ_D was necessary to describe the transients. Fig. 8 shows that while τ_C is approximately constant over a wide range of on/off and gate–drain voltages, τ_D has strong exponential dependence on both on-state gate–source and drain–source voltages, possibly due to impact ionization or field-induced barrier lowering under high voltages. Fig. 9 shows that $\Delta I_{\rm DS}$ is dependent mainly on the drain–source voltage, as well as the difference between on- and off-state gate–source voltages. These results show that $i_{\rm DS}$ can be expressed as follows in (3), which is also sufficiently compact for circuit simulation use:

$$i_{\rm DS} = I_{\rm DS}(V_{\rm DS}, V_{\rm GS}) - \Delta I_{\rm DS}\left(V_{\rm DS}, V_{\rm GS} - V_{\rm GS}^{\rm OFF}\right) \cdot \left(1 - e^{-t_{\rm OFF}/\tau_C}\right) \cdot \exp\left[-\frac{t}{\tau_D(V_{\rm GS}, V_{\rm DS})}\right]. \quad (3)$$

Using SPICE, a voltage-dependent current source may be used to model the drain current reduction, just as in the case of the epitaxial MESFET. However, since the drain–gate access resistance remains constant for the implanted MESFET, the parasitic linear MESFET is no longer needed [see Fig. 10(a)]. Notice that the characteristics of $\Delta I_{\rm DS}$ (Fig. 9) are very similar to the drain characteristics of a typical MESFET. Therefore, the parasitic current source is modeled as another MESFET. Time-dependent control of the current source is provided by a nonlinear RC subcircuit with the detrapping time constant modeled by a voltage dependent resistor [see Fig. 10(b)]. With unity capacitance, $R_C = \tau_C$ and $R_D = \tau_D = \tau_0 \exp(\gamma V_{\rm GS} + \delta V_{\rm DS})$, where τ_0, γ, and δ are fitting constants. The subcircuit is driven by the instantaneous gate–source voltage. The instantaneous voltage across the capacitor is then used to control the current source. Once again, the intrinsic MESFET is simulated by a conventional model using the steady-state drain characteristics.

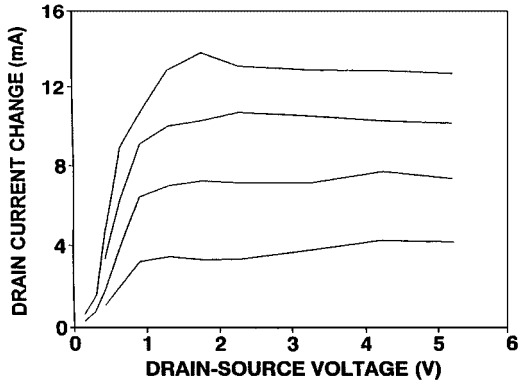

Fig. 9. Extracted drain current changes in the implanted MESFET after the gate voltage was pulsed from -6, -5, -4, or -3 (top down) to -0.25 V. The dependence of the drain current changes on the drain–source voltage and the difference between on- and off-state gate–source voltages has a similar form to typical MESFET characteristics and is modeled as such.

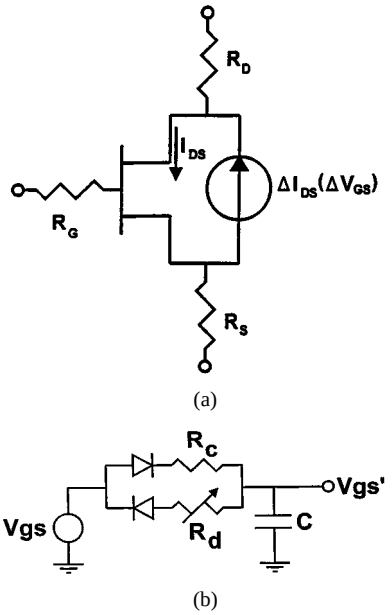

Fig. 10. Circuit model implemented in SPICE for the implanted MESFET. (a) The parallel current source is modeled as an MESFET and is used to mimic threshold voltage shifts. (b) A nonlinear RC timing circuit is used to drive parallel current source. The voltage dependence of the detrapping time constant is modeled with a variable resistor.

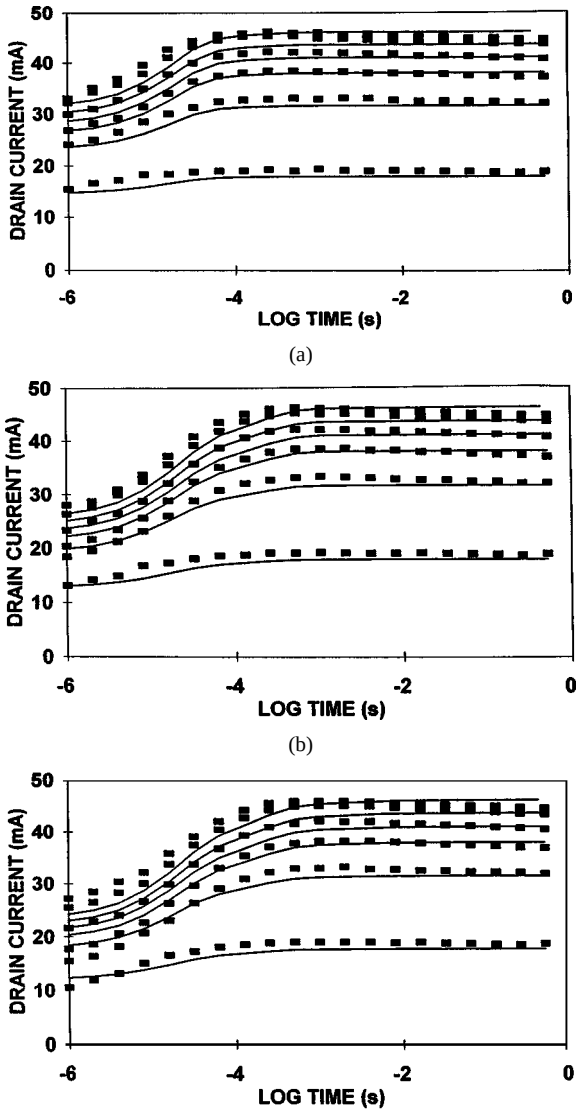

Fig. 11. (■) Measured and (—) simulated drain current transients of the epitaxial MESFET for off times of: (a) 0.1, (b) 1, and (c) 10 ms. On- and off-state gate–source voltages are 0.5 and −4 V, respectively. Drain supply equals 0.5, 1.0, . . ., 3.0 V bottom up.

III. Model Verification

For model verification, pulsed *I–V* characteristics after various combinations of off voltages, and times were simulated and compared to that measured on an epitaxial MESFET (Fig. 11) and an implanted MESFET (Fig. 12). To verify the models further, additional experiments were run. In the first experiment, an epitaxial MESFET was normally biased off for sufficient time to ensure a steady off state. It was then pulsed on, with a 7-kHz 1.5-V signal superimposed on the pulse (Fig. 13). In the second experiment, an epitaxial MESFET was normally biased on to ensure a steady on state. It was then pulsed down to partially off, with a 100-kHz 1.25-V signal superimposed on the pulse (Fig. 14). In the third experiment, a normally off (gate–source voltage $= -3$ or -6 V) implanted MESFET is pulsed on (gate–source voltage $= -1.25$ V) with a 10-kHz 1.75-V signal superimposed on the pulse (Fig. 7). In all three

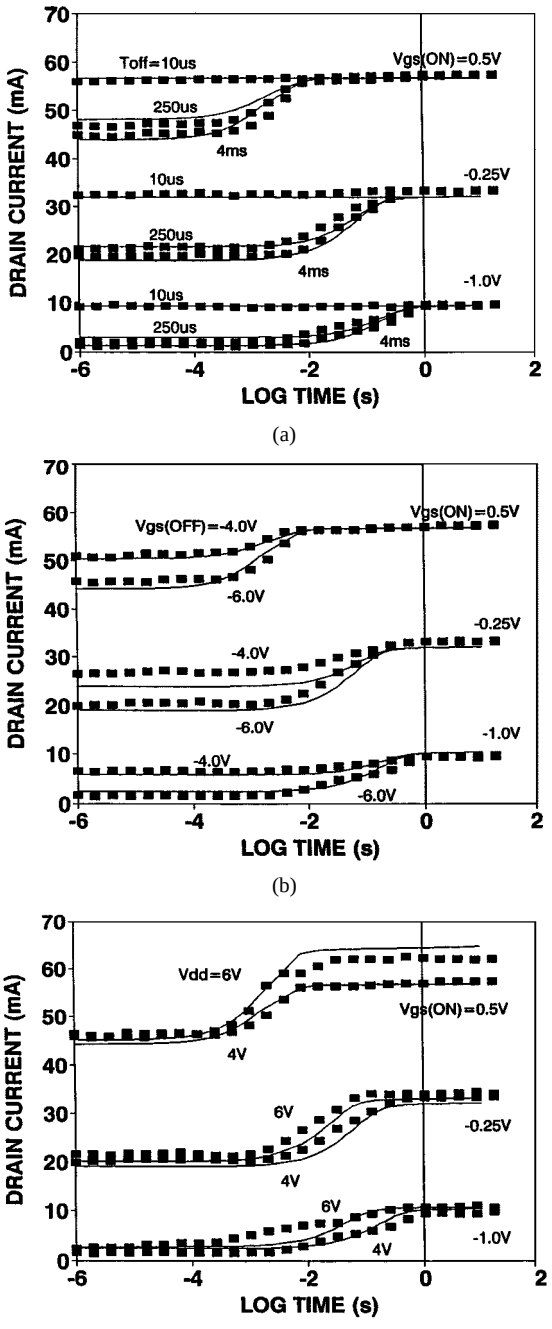

Fig. 12. (■) Measured and (—) simulated drain current transients of the implanted MESFET showing their dependencies on: (a) off time, (b) off-state gate–source voltage, and (c) drain supply. When not varied, off time $= 1$ ms, off-state gate–source voltage $= -6$ V, and drain supply $= 4$ V. On-state gate–source voltage $= 0.5, -0.25$, and -1.0 V top down.

experiments, the simulated results compare well with the measured data.

IV. Discussion

The success of the present model in simulating the transient behavior of a MESFET after various historical events is primarily owing to the use of both trapping and detrapping time constants. While the general supposition has been that the trap effect on the high-frequency characteristics is determined by the average voltages near the quiescent point [1], the above mea-

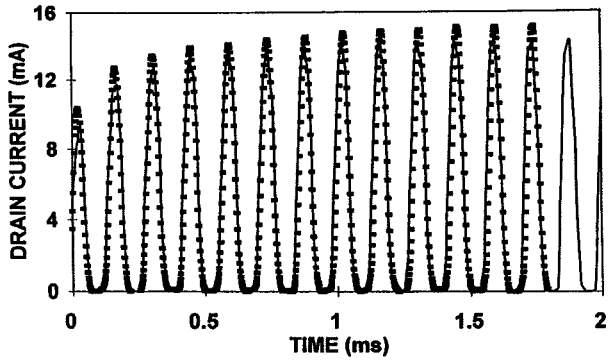

Fig. 13. (■) Measured and (—) simulated drain current response of a normally off epitaxial MESFET to a gate pulse with a 7-kHz 1.5-V signal superimposed on the pulse, as in the case of Fig. 2.

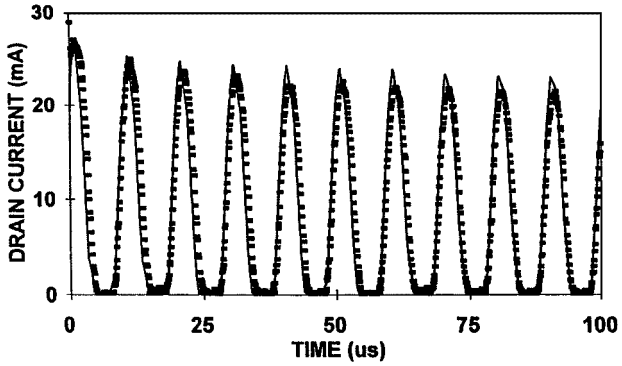

Fig. 14. (■) Measured and (—) simulated drain current response of a normally on epitaxial MESFET to a gate pulse of 1 to −1 V with a 100-kHz 1.25-V signal superimposed on the pulse.

surements and simulations show that this supposition is not necessarily valid. This is because the steady-state trap density is dependent on a balance between trapping and detrapping, which tend to occur at peak RF swings. In fact, as illustrated with the epitaxial MESFET, in some cases, the extreme voltages are more consequential than the average voltages.

While verification has been performed at rather low frequencies, the general agreement between the simulated and measured results at these frequencies indicate that the model will be capable of predicting the transient of typical RF carriers. Simulating the transient of RF waveforms is computationally intensive due to the large differences between RF periods and trapping/detrapping times. By using an ac period, approximately one-tenth of the fastest trapping/detrapping time and by properly scaling the capacitances and inductances, it is possible to achieve good agreement between the simulated ac response and the RF waveforms sampled at the same ac frequency, effectively aliasing RF with ac.

V. Conclusion

A phenomenologically based transient SPICE model was developed to account for the charging and discharging of traps in GaAs MESFETs. Epitaxial MESFETs, which are sensitive to surface traps, and ion-implanted MESFETs, which are sensitive to substrate traps, were both modeled. While there are differences in the models, which stem from the trap locations, the effects of both types of traps are easily simulated. The ability to mimic trapping/detrapping through nonlinear RC circuits allows both low-frequency dispersion and gate–lag characteristics to be simulated simultaneously. With this flexibility, the model has been able to duplicate pulsed ac signals, a first step in simulating the transient of RF carrier waveforms under digital modulation. Finally, this paper has illustrated the possibility of efficiently modeling an RF device for its instantaneous state, which, in general, is not only dependent on the instantaneous state variables, but also the path and speed through which the instantaneous state variables are arrived at.

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